DS1336
Afterburner Chip

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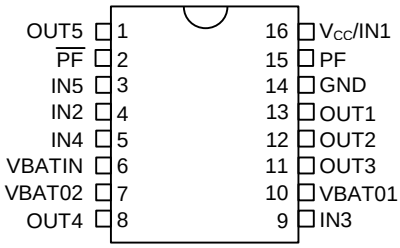
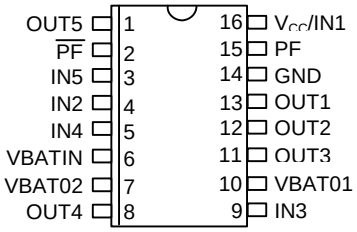
FEATURES

- Provides power switching of up to 1.5 amps at voltages between 3.0 and 5.0 volts
- Five separate power switches
- Selectable battery switches for use with
- battery-backed systems
- Very low on impedance of 0.7O
- Battery backup current of 4 mA
- Diode-isolated battery path
- Available in 16-pin DIP or 16-pin SOIC surface
- mount package
- Low voltage drop battery path
- Connects directly to a variety of Dallas Semiconductor devices, adding increased switching capability for large battery backup current applications

PIN ASSIGNMENT



16-Pin DIP (300-mil)
See Mach. Drawings Section



16-Pin DIP SOIC (300-mil)
See Mach. Drawings Section

PIN DESCRIPTION

V_{CC}/IN1	- +5V Input and Input 1
IN2 - IN5	- Inputs 2 - 5
OUT1 - 5	- Outputs 1 - 5
V_{BATIN}	- External Battery Input
V_{BAT01}	- Diode Protected Battery Output
V_{BAT02}	- Low Voltage Drop Battery Output
PF, $\overline{PF}$	- Power-fail Inputs
GND	- Ground

DESCRIPTION

The DS1336 Afterburner Chip is designed to provide power switching between a primary power supply (V_{CC}) and a backup battery power supply (V_{BAT}). Five V_{CC} and two battery paths are provided which can be used individually or in parallel to supply uninterrupted power in applications such as SRAM networks. When used with one of the Dallas power monitoring devices listed in Table 1, the DS1336 allows a load to be switched from its main power supply V_{CC} to a battery backup supply when V_{CC} falls out of tolerance. A user may selectively tie together any combination of the output pins to provide the desired high current supply, providing up to 300 mA per OUT pin or a maximum of 1.5A. Depending upon the user's backup supply load requirements, either of the V_{BAT} outputs may be tied to the OUT pins to supply

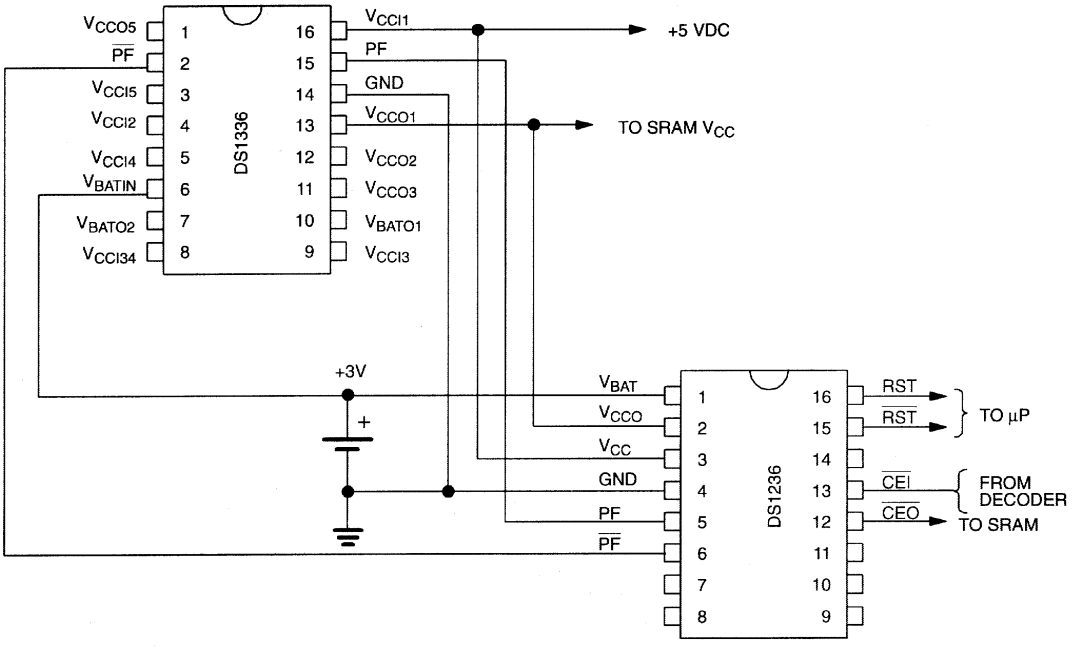
current when V_{CC} is out of tolerance. The DS1336 switches back to the higher current V_{CC} from battery current when PF and $\overline{PF}$ become inactive.

OPERATION

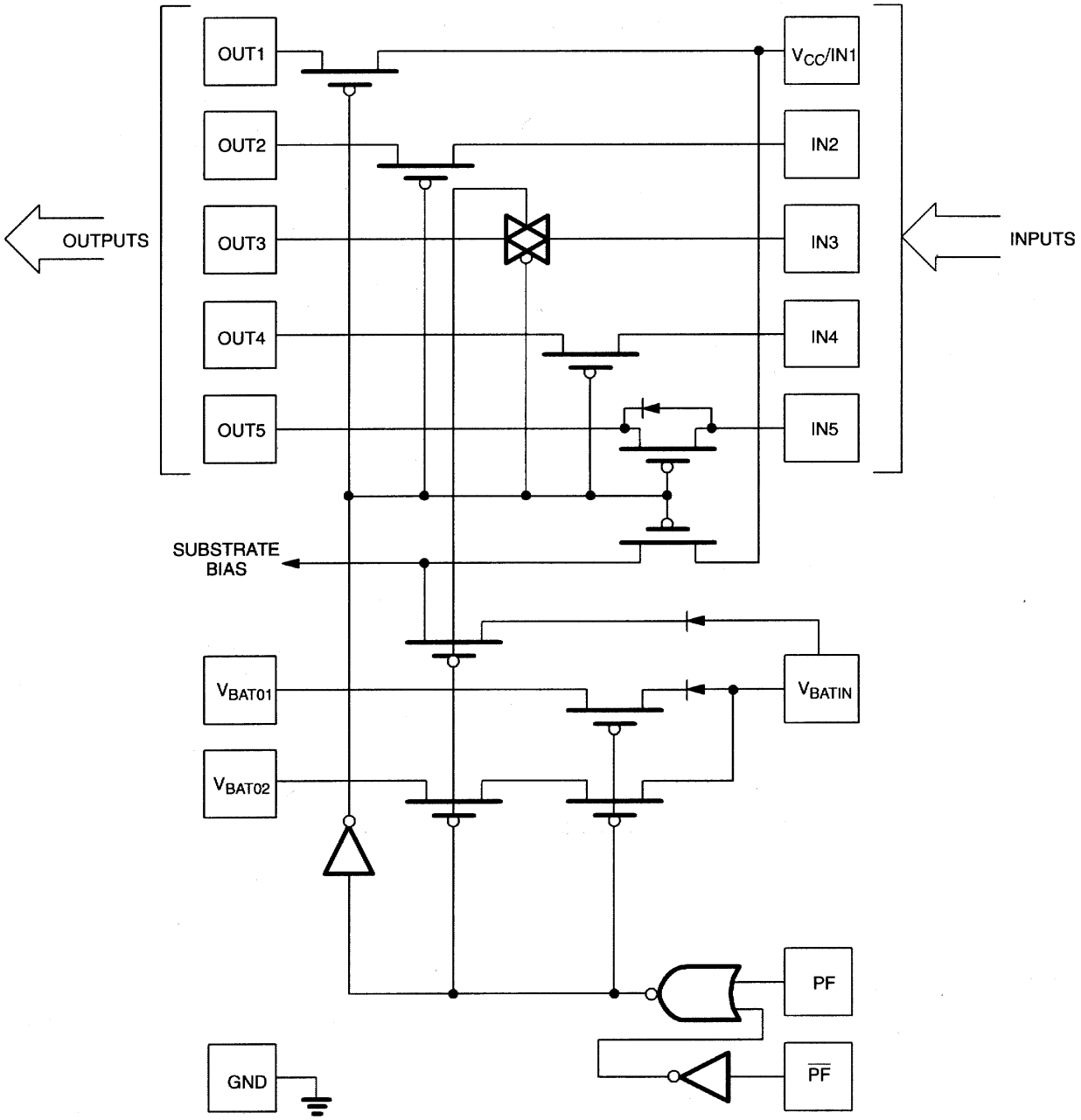
The required PF or $\overline{PF}$ input which controls the switching between the main V_{CC} and backup battery can be supplied by any of the devices listed in Table 1. All of the devices provide the DS1336 with a PF or $\overline{PF}$ signal, switching between a main supply V_{CC} and backup supply V_{BAT} when V_{CC} falls out of tolerance. For applications requiring switching from the V_{CC} supply inputs to V_{BAT}, the required PF or $\overline{PF}$ input to the DS1336 can be provided by the DS1236, DS1239, DS5001, or DS5340. For applications requiring switching from the V_{CC} inputs to the V_{BAT} input when V_{CC} begins falling out of tolerance, any of the Dallas Semiconductor devices listed in Table 1 can provide the DS1336 with the required switching input. A typical application is shown in Figure 1. For applications where switching between V_{CC} and V_{BAT} must occur at a voltage level such that V_{CC} is still greater than V_{BAT}, the OUT5 pin is recommended as it provides a diode path which will provide for a gradual transition between V_{CC} and V_{BAT}. OUT5 can be tied to the other OUTPUT pins to provide a gradual transition for all five current paths. In applications where tri-state switching is desired, OUT5 should be omitted. Only the PF/$\overline{PF}$ pin is required for switching. In cases where the PF input will not be used, it should be connected to GND.

When either PF or $\overline{PF}$ is active, either of the V_{BAT0X} outputs is available, although they should not be tied together (Figure 2, "DS1336 Block Diagram"). V_{BAT01} is recommended for sensitive applications such as providing backup current to timekeepers, because its diode isolated path provides for increased protection. V_{BAT02} is not recommended for applications where it would be tied to an OUTPUT pin supplying a voltage greater than that of the backup battery because V_{BAT02} is not a diode isolated current path.

TYPICAL APPLICATION Figure 1



DS1336 BLOCK DIAGRAM Figure 2



DALLAS SEMICONDUCTOR DEVICES WHICH PROVIDE PF OR $\overline{PF}$ INPUT TO NIL Table 1

DEVICE	SWITCH > V_{BAT}	SWITCH AT V_{BAT}	DEVICE	SWITCH > V_{BAT}	SWITCH AT V_{BAT}
DS1211	X		DS1238	X	X
DS1212	X		DS1239	X	X
DS1231	X		DS1259	X	
DS1232	X		DS1260	X	
DS1233	X		DS1610	X	
DS1233A		X	DS1632	X	
DS1233D	X		DS1833	X	
DS1234	X		DS5001	X	X
DS1236	X	X	DS5340	X	X
DS1237	X				

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC OPERATING CONDITIONS (t_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC1}	3.0	5.0	5.5	V	1
Supply Current	I_{CC1}		0.25	1.0	mA	
Supply Current	I_{CC2}		50	100	nA	3
Input Low Voltage	V_{IL}			0.8	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}	V	1
Current Output $V_{CC}=V_{CC1}$, PF=0, $\overline{PF}$=1	I_{CCO}			300	mA	2
Current Output V_{CC}=0, PF=1, $\overline{PF}$=0	$I_{BAT01-2}$			4.0	mA	4
Current, Forward Bias of V_{CC5} Diode	I_{FB}			20	mA	
Off Impedance	R_{OFF1}	5.0			MΩ	5
Off Impedance	R_{OFF2}	10			MΩ	6
On Impedance	R_{ON1}			0.7	Ω	7
On Impedance	R_{ON2}			50	Ω	8

AC CHARACTERISTICS (t_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay	t_{PD}		10		ns	9
Switch Delay Power-fail	t_{PF}		100		ns	
Switch Delay Power-on	t_{PON}			100	ns	
Capacitance PF, $\overline{PF}$	C_I			7	pF	

NOTES:

1. All voltages referenced to ground.

2. I_{CCO} with a voltage drop of 0.2 volts from any V_{CCO} output.

3. V_{CC}=0, V_{BATIN}=3.0 volts.

4. V_{BAT01} with a voltage drop of 1.0 volts.

5. R_{OFF1} applies to $V_{CCO1, 2, 3, 4}$.

6. R_{OFF2} applies to $V_{BATO1, 2}$.

7. Applies to V_{CCO1-5}, 300 mA.

8. Applies to $V_{BATO1-2}$, 4 mA.

9. V_{CCI3} to V_{CCO3} delay when used as chip enable control for write protection of a memory device. In this application a current 8 mA source current on V_{CCI3} with 50 pF load on V_{CCO3} can be accommodated.